REMARKS

The Examiner rejected claims 1-3, 5-6, 8-9, 23-25, 27-28 and 30-31 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,133,062 (***Joshi***). Applicant respectfully traverses this rejection.

Applicant respectfully asserts that ***Joshi*** does not teach, disclose, or suggest all of the elements called for by claim 1 of the present invention. ***Joshi*** discloses a controller that is directed to control address signals of a RAM buffer. The controller disclosed by ***Joshi*** is directed to simulate the operation of first-in-first-out (FIFO) registers in a memory buffer. In contrast to ***Joshi***, claim 1 (as amended) of the present invention calls for receiving data from an external source and decoding the data to determine whether to *wake up* a host circuitry from a *sleep mode*. In contrast, ***Joshi*** calls for addressing registers in a memory buffer that are contained *within* a host circuitry; whereas claim 1 of the present invention is concerned with *waking up the host circuitry* from a sleep mode based upon decoding and comparing incoming data. ***Joshi*** does not call for transitioning a host circuitry from a sleep mode to a wake-up mode based upon decoding and comparing incoming data.

As an example of how ***Joshi*** does not teach various elements of claim 1, the Examiner cited lines 32-35 of col. 11 in ***Joshi*** to illustrate the element of determining whether the received data signals should be received by the host circuitry. Applicant respectfully disagrees. The boundary comparator 88 in ***Joshi*** merely generates a control signal to indicate when the currently selected pointer had reached an ending address of a FIFO in the buffer memory (see col. 11, lines 29-35). This is merely indicating that the end of a range of addresses in a register in a buffer memory has been reached. This does not suggest anything regarding making a determination that the received data signals should be received by the host circuitry.

As another example, the Examiner cited column 11, line 43 through column 12, line 9 to illustrate the element of waking up the host circuitry based upon a determination that the data is addressed to the host circuitry. Applicant respectfully disagrees. This cited portion of ***Joshi*** merely refers to decoding instructions from the node processor and generating a chip select signal to address a particular RAM buffer in the host circuitry (see col. 11, line 43 - col. 12, line 9). ***Joshi*** is referring to addressing particular buffer memory space within a host circuitry. In contrast, an element of claim 1 calls for waking up the host circuitry itself from a sleep mode based upon received data, which is distinct from merely asserting a chip select signal, as disclosed by ***Joshi***. For the various reasons cited above, ***Joshi*** is mainly concerned with addressing memory space within a host circuitry, wherein claim 1 of the present invention calls for waking up a host circuitry from a sleep mode based upon received data. Therefore, claim 1 (as amended) of the present invention is allowable. Additionally, for at least the reasons cited above, claim 23, which has similar elements as claim 1, is also allowable.

Independent claims 1 and 23 are allowable for at least the reasons stated above. Dependent claims 2-9, which depend from independent claim 1, and claims 24-31, which depend from independent claim 23, are also now considered to be patentable in light of the above-presented arguments.

The Examiner rejected claims 10-22 under 35 U.S.C. § 103(a) as being unpatentable over ***Joshi*** (U.S. Patent 5,133,062) in view of U.S. Patent No. 5,822,550 (***Milhaupt***). Applicant respectfully traverses this rejection.

Adding the disclosure of ***Milhaupt*** to ***Joshi*** would not produce all of the elements called for by claim 10, as amended, of the present invention. The Examiner cites ***Milhaupt*** to provide the elements of a clock divider, as mask circuitry, a counter, status registers, and clock register.

However, in addition to these elements, ***Joshi*** is also missing the element of a host circuitry that is capable of entering a wake up state from a sleep mode based upon received data, as called for by claim 10 (as amended) of the present invention. Neither ***Joshi*** nor ***Milhaupt*** discloses a host circuitry that is capable of entering a wake up state from a sleep mode based upon received data, as called for by claim 10. Therefore, combining ***Joshi*** and ***Milhaupt*** would not produce all of the elements of claim 10. In other words, the elements of claim 10 that are missing from ***Joshi*** are not disclosed by ***Milhaupt***, therefore, combining them would not result in all of the elements called for by claim 10 (as amended).

Additionally, Applicant respectfully asserts that one of ordinary skill in the art would not have motivation to combine the teachings of ***Joshi*** and ***Milhaupt***. ***Joshi*** discloses a controller that is directed to control address signals of a RAM buffer. ***Milhaupt*** is directed towards a single-chip integrated circuit that has an interface for coupling two data paths, wherein the first data path is related to external pin states and the second data path is related to internally generated data. Even though ***Joshi*** and ***Milhaupt*** are related to electronic circuits, an invention directed to controlling address signals of a RAM buffer is in a different realm from the integrated chip with the interface described above. Therefore, without impermissible hindsight, a person with ordinary skill in the art would not be motivated to combine the teachings of ***Joshi*** and ***Milhaupt*** to produce the subject matter called for by claim 10. However, as described above, even if ***Joshi*** and ***Milhaupt*** were combined, all of the elements of claim 10 (as amended) would not be disclosed. Therefore, Applicant respectfully asserts that claim 10 is allowable.

Independent claim 10 is allowable for at least the reasons stated above. Dependent claims 11-22, which depend from independent claim 10 are also now considered to be patentable in light of the above-presented arguments.

Modifications have been made to claim 3 and claims 24-31 to correct typographical and/or form errors.

Additionally, new claims 32-34 have elements that are directed to waking up a host circuitry from a sleep mode based upon received data. Therefore, for at least the reasons cited above, newly added claims 32-34 are also allowable.

In light of the arguments presented above, Applicant respectfully asserts that claims 1-34 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

A Submission of Formal Drawings is submitted to correct informalities of Figure 4.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069 to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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MARKED-UP CLAIMS

1. (Amended) A method for detecting and decoding data comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

3. (Amended) The method as described in claim 2, wherein said step of detecting a size of said received set of data signal and decoding said received set of data signals, comprises:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a [member] number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

10. (Amended) An apparatus for detecting and decoding data, comprising:

a data formatter;

a clock divider;

a counter;

a host circuitry interface capable of transmitting and receiving data from a host circuitry, said host circuitry enter a wake up state from a sleep mode based upon data received by said host circuitry;

a memory circuitry;

a plurality of comparators;

a mask circuitry;

a digital logic circuitry;

a plurality of status registers; and

a plurality of clocked registers.

23. (Amended) A [computer program for detecting and decoding data comprising] computer readable program storage device encoded with instructions that, when executed by a computer, performs a method, comprising:

receiving a set of data signals from an external data source;

detecting a size of said received set of data signals;

decoding said received set of data signals;

extracting a destination address from said set of data signals;

comparing said destination address extracted from said data signals to a known data value;

determining whether said received data signals should be received by a host circuitry based upon said comparison of said destination address extracted from said data signals to a known data value;

generating at least one status signal alerting said host circuitry of said determination that said received data signals should be received by said host circuitry; and

waking up said host circuitry from a sleep mode upon a determination that said received set of data is addressed to said host circuitry.

24. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said set of data signal received is a data packet that is in a serial data format, over a network line.

25. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 24, wherein said step of detecting a size of said received set of data signal and decoding said received set of data signals, further comprises:

converting said serial data packet into a parallel data format;

extracting a word clock from said received data packet;

incrementing a [member] number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry; and

inputting a set of data signals from said memory circuitry into an appropriate comparator.

26. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said act of extracting a destination address from said set of data signals further comprises slicing said parallel data such that at least one destination address data word is generated.

27. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 25, wherein said method of comparing said destination address to a known data value further comprises:

performing a comparison function upon said converted, parallel set of data signals, and said set of data from said memory circuitry;

generating a digital comparator status signal in response of said performance of comparator function; and

clocking in said digital comparator data signal into a register.

28. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 27, wherein said method of determining whether said received data signals should be received by a host circuitry further comprises latching all output of said plurality of comparators into a digital logic circuitry.

29. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said output of said comparators are not latched when a mask circuitry indicates that a particular frame of data is not compared.

30. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 28, wherein said method of generating a status signal alerting said host circuitry further comprises performing an OR function upon all said latched output of said comparators.

31. (Amended) The [computer program as described] computer readable program storage device encoded with instructions that, when executed by a computer, performs the method described in claim 23, wherein said method of waking up said host circuitry further comprises generating a status signal alerting said host that a address match has been found.

32. (New) A method, comprising:

receiving a data signal;

extracting a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address; and

waking up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

33. (New) The method of claim 32, wherein extracting said destination address further comprises:

converting a serial data packet from said received data into a parallel data format;

extracting a word clock from said received data packet;

incrementing a number held by said counter, said word clock generating a word count;

inputting said converted parallel format data into a plurality of comparators;

using said word count to address data stored in a memory circuitry;

inputting a set of data signals from said memory circuitry into an appropriate comparator; and

extracting said destination address by slicing said parallel data such that at least one destination address data word is generated.

34. (New) An apparatus, comprising a controller to receive a data signal, extract a destination address based upon said data signal to determine whether a host circuitry is being addressed by comparing said destination address to a predetermined address, and wake up a host circuitry from a sleep mode based upon said determination that said host circuitry is being addressed.

35. (New) The apparatus of claim 34, further comprising:

a data formatter capable of converting a serial stream of data into parallel data words and detecting an end of a data stream;

a counter to receive parallel formatted data from said data formatter;

a clock divider capable of incrementing a count held by said counter;

a memory circuitry comprising a memory element and a memory data access logic;

a plurality of comparators to receive parallel formatted data from said data formatter;

a plurality of clocked registers;

a mask circuitry capable of preventing a registering of said comparator output into said clocked registers; and

a plurality of status registers to latch an output from said comparators.